REMARKS

Reconsideration of the present application is respectfully requested. Claims 1-43 have been canceled. Claims 44-62 are newly added. No new matter has been added.

The claims have been amended to better set forth the features which Applicant regards as most important to protect, not in response to the rejections. These features include:

1) the processor has a multi-level hierarchical instruction set;

2) the outputs of specific functional units (e.g., multiplier, ALU) can be explicitly referenced by instructions defined from the processor's instruction set.

These features reflect a novel and non-obvious architecture and programming model that enable the processor to be extremely fast and efficient at processing graphics and image data.

Note that the new claims do not add new matter. Each of these features is adequately described (per 35 U.S.C. § 112, first paragraph) in Applicant's description as originally filed. Feature "1)" in the preceding paragraph is described at, for example, page 75 of the annex to the original specification (which formed part of the original disclosure), entitled, "IMAGINE: The Image Engine – Documentation & User's Manual," version 2.80.

Feature "2)" noted above is supported, for example, in the substitute specification at page 3 lines 4-8 and page 8 lines 17-19, and also in the annex at page 73, center of left column, and at page 71, left column.

Turning now to the claims, claims 26-43 were under 35 U.S.C. § 103(a) based on U.S. Patent no. 5,465,224 of Guttag et al. ("Guttag"). Those claims have been canceled, rendering the rejection moot. Therefore, reference is now made to the new claims.

Independent claim 44 recites a processor which has an instruction set, where the instruction set has a hierarchy of instruction levels. Guttag does not disclose or suggest a processor that has an instruction set with a hierarchy of instruction levels, nor would this be obvious in view of Guttag or the other art of record. Regardless, claim 44 also recites that the plurality of hierarchical instruction levels include both a RISC/CISC assembly code level *and* a free pipeline assembly code level. Guttag also fails to disclose or suggest these features. Neither is Applicant aware of these features being disclosed or suggested anywhere else in the prior art. Therefore, claim 44 and all claims which depend on it are patentable over the cited art.

Independent claim 51 recites a processor which comprises a plurality of functional units, including a multiplier unit and an arithmetic logic unit, wherein each of the plurality of functional units has an output that can be explicitly referenced in instructions defined from the instruction set of the processor. Guttag does not disclose or suggest a processor with such features, nor would this be obvious in view of Guttag or the other art of record. Neither is Applicant aware of these features being disclosed

or suggested anywhere else in the prior art. Therefore, claim 51 and all claims which depend on it are patentable over the cited art.

Independent claim 58 recites limitations similar to those discussed above, and other limitations. Therefore, claim 58 and all claims which depend on it are also patentable over the cited art, for similar reasons.

Dependent Claims

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicants' silence regarding any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

Conclusion

For the foregoing reasons, the present application is believed to be in condition for allowance, and such action is earnestly requested.

If any additional fee is required, please charge Deposit Account No. 02-2666.

Respectfully submitted,
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